WHAT IS CLAIMED IS:

Sub A7

1. A method comprising the steps of:

receiving a minimum number of needed power bond pads;

determining a first number of power bond pads to be implemented, wherein the first number of power bond pads is greater than or equal to the minimum number; and

determining a second number of active buffer areas to be implemented for the power bond pads, wherein the second number is less than the first number.

2. The method of claim 1, further comprising the step of:

specifying a placement of a third number of immediately adjacent bond pads within a first distance along a periphery of a die, wherein the third number is less than the first number;

specifying a placement of a fourth number of immediately adjacent active buffer regions within the first distance along the periphery of the die, wherein the fourth number is less than the third number.

3. The method of claim 2, further comprising the step of:

specifying a placement of a trace connecting two bond pads of the immediately adjacent bond pads, wherein the two bond pads are not immediately adjacent to each other.

4. The method of claim 3, wherein the step of specifying the placement of the trace includes the placement of the trace being at least partially between the two bond pads and an outer periphery of a die.

5. A method comprising the steps of:

connecting a first bond pad to a first portion of a package, wherein the first portion of the package is to supply a predetermined voltage;

connecting a second bond pad to a second portion of a package, wherein the second portion of the package is to supply the predetermined voltage; and

wherein the first bond pad is connected to the second bond pad, and exactly one of the first bond pad and second bond pad is connected to an active buffer region, and a third bond pad is immediately adjacent to the second bond pad and to the first bond pad.

6. The method of claim 5, wherein the first portion of the package and the second portion of the package are electrically connected.

7. The method of claim 1, wherein a first pitch between the first bond pad and the third bond pad is less than an average pitch between buffers in the active buffer region.

8. The method of claim 1, wherein a first pitch between the first bond pad and the third bond pad is the same as a second pitch between the second bond pad and the third bond pad.

9. The method of claim 8, wherein the first pitch is a minimum allowable pitch.

10. The method of claim 8. wherein a fourth bond pad is immediately adjacent the second bond pad, and a third pitch between the second bond pad and the fourth bond pad is equal to the first pitch.

11. The method of claim 10, wherein the first pitch is a minimum allowable pitch.

12. The method of claim 8, wherein a fourth bond pad is immediately adjacent to the second bond pad, and a third pitch between the second bond pad and the fourth bond pad is different than the first pitch.

13. The method of claim 12, wherein the first pitch is a minimum allowable pitch.

14. An apparatus comprising:

semiconductor substrate having an input output (IO) ring, the IO ring having a bond pad portion and an active buffer portion;

the bond pad portion including:

a first bond pad;

a second set of bond pads having one or more bond pads;

a third bond pad, wherein the second set of bond pads is immediately adjacent to the first and third bond pads; and

a conductive trace coupling the first bond pad to the third bond pad.

15. The apparatus of claim 14, wherein the first bond pad and the third bond pad are power pads, wherein a power pad is to be coupled to a fixed voltage source.

16. The apparatus of claim 15, wherein the fixed voltage source is one of Vdd and Vss.

17. The apparatus of claim 14, further comprising:

a package substrate having a power portion, wherein the power portion is to provide a fixed voltage;

a first bond wire connected to the first bond pad and the power portion;

a second bond wire connected to the third bond pad and the power portion.

18. The apparatus of claim 17 further comprising exactly one of the first bond pad and the third bond pad being connected to the active buffer portion of the IO ring.

19. The apparatus of claim 14, wherein the second set of bond pads includes one bond pad.

20. The apparatus of claim 14, wherein the second set of bond pads includes more than one bond pads.